

App. Serial No. 10/527,569
Docket No.: NL020843 US

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In the Claims:

This listing of claims replaces all prior versions.

1. (Original) A method for testing quality of semiconductor devices on a wafer, the method comprising the steps of:
generating quality test-data for a limited number of semiconductor devices on the wafer,
deciding based on the generated quality test-data whether other semiconductor devices on the wafer are to be tested, or not to be tested,
based on the result of the deciding step, testing or not testing the other semiconductor devices on the wafer, and
if some semiconductor devices have not been tested, selecting at least one non-tested semiconductor device on the wafer for further processing.
2. (Original) A method according to claim 1, wherein the deciding step is a step of automatically deciding based on a comparison of a yield calculated from the generated quality test-data, with a pre-set value.
3. (Original) A method according to claim 1, wherein the limited number of semiconductor devices are located on the wafer as determined by a spatial pattern.
4. (Original) A method according to claim 3, wherein the pattern comprises a pattern selected from one or more of a circular pattern, an X-cross pattern, a pattern in the form of a plus-sign, a spiral pattern.
5. (Original) A method for testing quality of semiconductor devices on a plurality of wafers, the method comprising the steps of:
generating quality test-data for a limited number of semiconductor devices on a number of wafers from the plurality of wafers,
deciding, based on the generated quality test-data, for each of the tested wafers, whether other semiconductor devices on the tested wafers are to be tested, or not to be tested,

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based on the result of the deciding step, testing or not testing the other semiconductor devices on the tested wafers, and

if some semiconductor devices have not been tested, selecting at least one non-tested semiconductor device on the wafer for further processing, wherein the limited number of semiconductor devices on each of the wafers are located on the wafers as determined by a spatial pattern, the spatial pattern being such that, by shifting it between wafers, a substantially complete wafermap can be obtained.

6. (Original) A method according to claim 5, wherein the shifting of the spatial pattern comprises a rotation of the spatial pattern.
7. (Original) A method for manufacturing a plurality of semiconductor devices on a wafer, one of the method steps comprising a step of quality testing according to any of the claims 1 or 5.
8. (Original) A wafer prober for testing a plurality of semiconductor devices on a wafer, the wafer prober comprising:
 - selecting means for selecting a limited number of the plurality of semiconductor devices on the wafer which will be tested,
 - at least one probe for measuring whether a selected semiconductor device meets at least one pre-set quality specification, the at least one probe generating quality test results,
 - deciding means for deciding, based on the quality test results, whether other semiconductor devices on the wafer are to be tested or not to be tested.
9. (Original) A wafer prober according to claim 8, wherein the at least one pre-set specifications is a design and/or performance specification.
10. (Original) A wafer prober according to any of claims 8 or 9, furthermore comprising a memory means for saving the generated test results.